Customer No.: 31561
Application No.: 10/710,933
Docket No.: 11537-US-PA

AMENDMENTS

In the Claims:

Claims 1-15 (cancelled)

Claim 16. (currently amended) A wafer-level package structure, comprising:

a silicon wafer substrate, having a plurality of identical sections, each section comprising:

a plurality of conductive blocks, disposed on the silicon wafer substrate~~and in each of the sections of the silicon wafer~~;

a dielectric layer covering the plurality of conductive blocks;

a metal interconnect layer disposed on the dielectric layer, ~~connecting the plurality of the conductive blocks, wherein~~ the metal interconnect layer comprising~~es at least via hole and~~ a plurality of pads disposed on an uppermost surface thereof, wherein the conductive blocks, the metal interconnect layer, and the pads are electrically connected by a plurality of vias~~the via hole electrically connects one of the conductive blocks and one of the pads, and wherein the pads are disposed on an uppermost surface of the metal interconnect layer~~; and

at least a chip, disposed on~~to each of the sections of the silicon wafer~~ the metal interconnect layer, wherein the chip includes a plurality of bonding pads that are correspondingly connected to the pads.

Claim 17. (currently amended) The wafer-level package structure of claim 16,

further comprising a passivation layer covering each section of the silicon wafer substrate.

Claim 18-27 **(cancelled)**